

SEGATM SERVICE MANUAL

GENESIS MEGA DRIVE PAL MEGA CD/SEGA CD

NO.	010
ISSUED	APRIL, 1994

CONTENTS

GENESIS VA7

PARTS SPECIFICATIONS 2

MEGA DRIVE PAL VA6.5

PARTS SPECIFICATIONS 11

MEGA CD / SEGA CD

PARTS SPECIFICATIONS 22

This manual contains IC specification to be added to the manuals issued previously.

Sega Enterprises, Ltd.

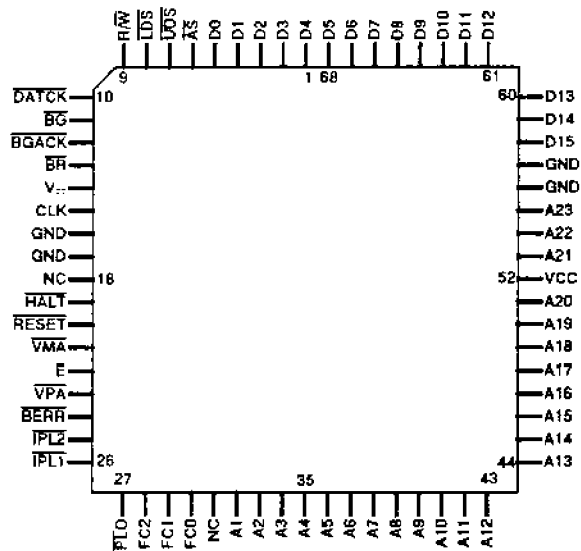
PARTS SPECIFICATIONS

IC1 16/32-bit Microprocessor

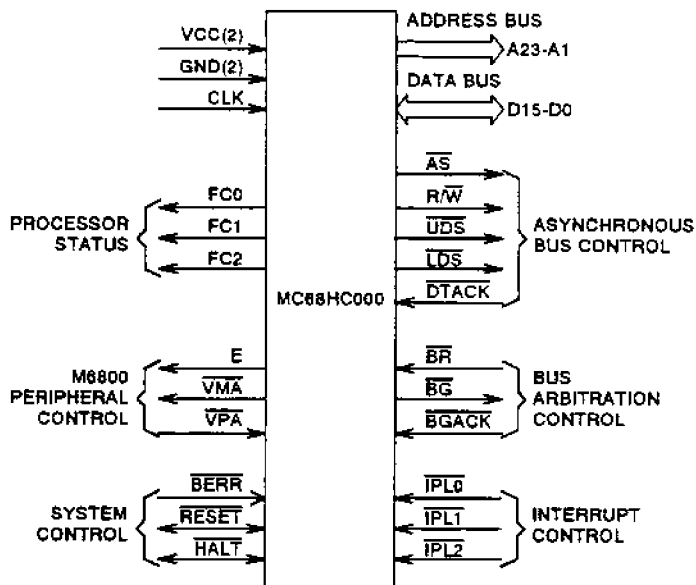
IC MC68HC000FN8

IC HD68HC000CP8

■ Top View & Pin Layout



■ Signal Description



■ Description

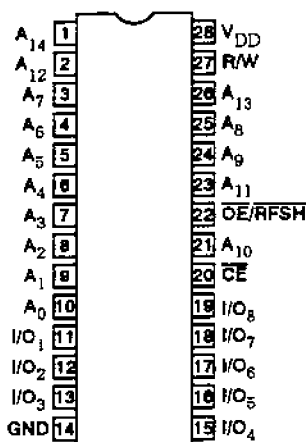
No.	Pin Name	I/O	Function	No.	Pin Name	I/O	Function	No.	Pin Name	I/O	Function
1	D ₄	I/O	Data bus	23	VPA	I	Valid peripheral address	46	A ₁₅	O	Address bus
2	D ₃			24	BERR	I	Bus error	47	A ₁₆		
3	D ₂			25	IPL ₂	I	Interrupt control	48	A ₁₇		
4	D ₁			26	IPL ₁			49	A ₁₈		
5	D ₀			27	IPL ₀			50	A ₁₉		
6	AS	O	Address strobe	28	FC ₂	O	Processor status	51	A ₂₀	O	Address bus
7	UDS	O	Upper data strobe	29	FC ₁			52	V _{CC}	—	Power supply
8	LDS	O	Lower data strobe	30	FC ₀			53	A ₂₁	O	Address bus
9	R/W	O	Read/Write	31	NC	—		54	A ₂₂	O	Address bus
10	DTACK	I	Data transfer Acknowledge	32	A ₁	O	Address bus	55	A ₂₃	O	Address bus
11	BG	O	Bus grant	33	A ₂			56	V _{SS}	—	GND
12	BGACK	I	Bus grant acknowledge	34	A ₃			57	V _{SS}	—	GND
13	BR	I	Bus request	35	A ₄			58	D ₁₅	I/O	Data bus
14	V _{CC}	—	Power supply	36	A ₅			59	D ₁₄		
15	CLK	I	Clock	37	A ₆			60	D ₁₃		
16	V _{SS}	—	GND	38	A ₇			61	D ₁₂		
17	V _{SS}	—	GND	39	A ₈			62	D ₁₁		
18	NC	—	Not connected	40	A ₉			63	D ₁₀		
19	HALT	I/O	Halt	41	A ₁₀			64	D ₉		
20	RES	I/O	Reset	42	A ₁₁			65	D ₈		
21	VMA	O	Valid memory address	43	A ₁₂			66	D ₇		
22	E	O	Enable	44	A ₁₃			67	D ₆		
				45	A ₁₄			68	D ₅		

IC2/3 32768 Word × 8bit CMOS Pseudo-Static RAM

IC HM65256BLFP-10

IC TC51832FL-10

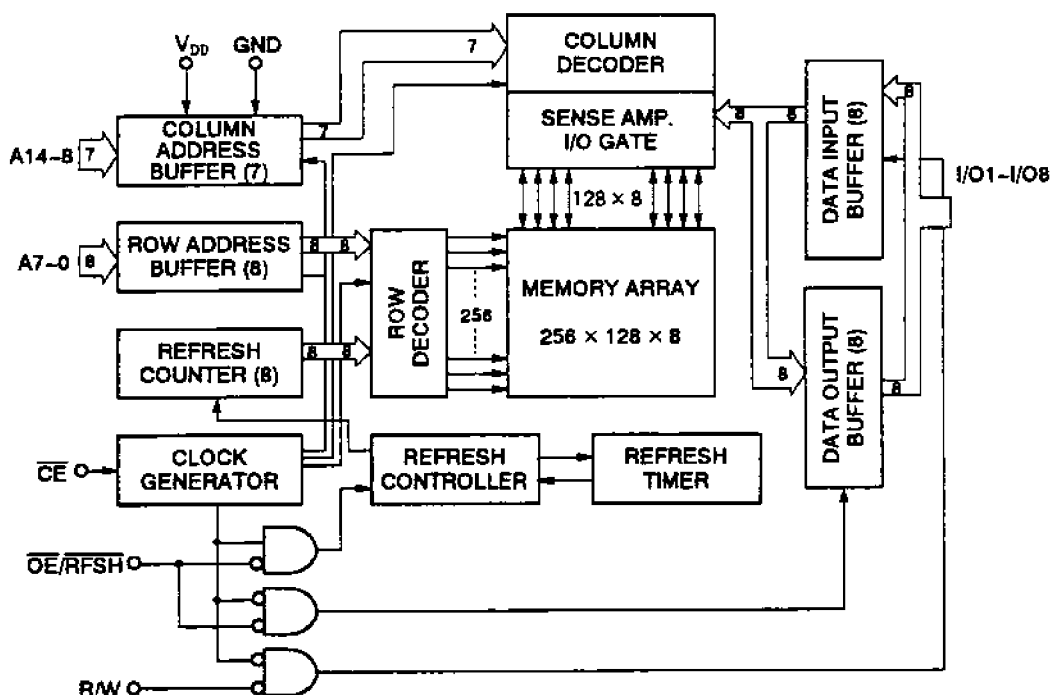
■ Top View & Pin Layout



■ Pin name

Pin Name	Function
A0~A14	Address input
R/W	Read/write input
$\overline{\text{OE/RFSH}}$	Output enable input/refresh input
$\overline{\text{CE}}$	Chip enable input
I/O1~I/O8	Data input/output
V _{DD}	Power supply
GND	Ground

■ Block Diagram

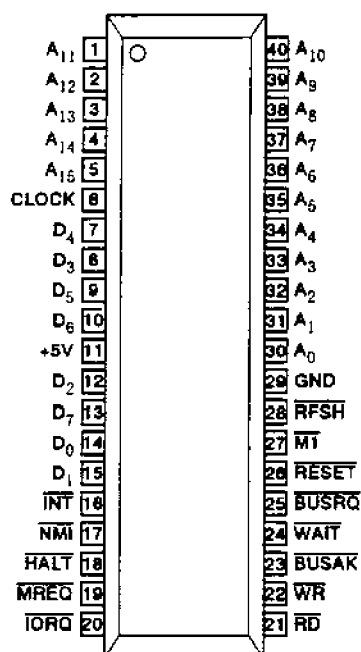


IC4 Z80A Central Processing Unit

IC Z80A

315-0041

■ Top View & Pin Layout



■ Description

Pin	Pin Name	I/O	Function
30~40 1~5	A0~A15	3-STATE O	System address bus.
15~12 7~10	D0-D7	3-STATE I/O	System data bus.
6	CLOCK	I	Receives a +5V single-phase clock signal.
16	INT	I	Active "Low". If the input/output device issues a signal that requests an interrupt to the Z80 CPU and the interrupt enable flag is zero, this interrupt request is accepted at the end of the instruction that is currently in progress.
17	NMI	I	Active "Low". This is an interrupt request that has priority over INT and cannot be inhibited by the software. NMI is always accepted, and when the instruction that is currently in progress finishes, interrupt processing is started and the Z80 CPU automatically starts from address 0066H.
18	HALT	O	Active "Low". This indicates that the HALT instruction is being executed. Executes the NOP instruction internally and also refreshes memory. The halt state is released by RESET, NMI or INT (when enabled).
19	MREQ	3-STATE O	Active "Low". This indicates that the address bus outputs the effective memory address for memory read/write.
20	IORQ	3-STATE O	Active "Low". This indicates that the low-order 8 bits of the address bus output effective addresses of the input/output device for the read/write operation with this device. This is output together with MI during an interrupt response to indicate the response.
21	RD	3-STATE O	Active "Low". This indicates the timing with which data from the memory or input/output device is read.
22	WR	3-STATE O	Active "Low". This indicates that the effective data to be written to the memory or input/output device the address of which is specified is on the data bus.
23	BUSAK	O	When the bus request is acknowledged, this informs the bus master which outputs the bus request that the system bus can be controlled.
24	WAIT	I	Active "Low". Signal to inform the CPU that the memory or input/output device the address of which is specified is not ready to send data. The CPU is waiting when this signal is input.
25	BUSRQ	I	Active "Low". This has priority over NMI and is accepted at the end of the machine cycle that is currently in progress. This is set to "Low" when a bus master other than the CPU wants to control the system bus.
26	RESET	I	Active "Low". This resets the interrupt enable flag, interrupt vector register and memory refresh register of the program counter to set the interrupt mode to mode 0, thus initializing the Z80 CPU.
27	MI	O	Active "Low". This indicates that the machine cycle being executed is an OP code fetch cycle.
28	RFSH	O	Active "Low". This indicates that the address for refreshing the dynamic RAM is output to the low-order 7 bits of the address bus. MREQ also goes "Low" at this time.

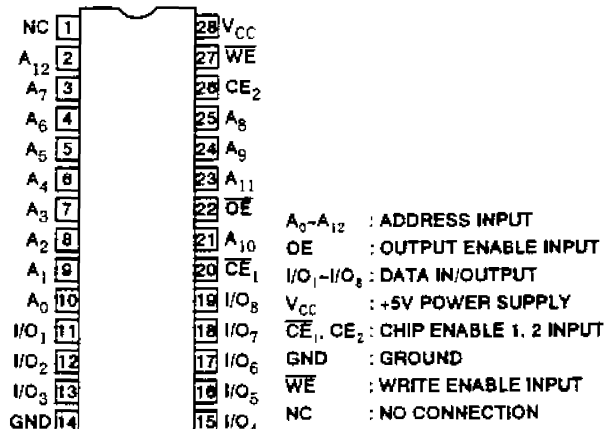
IC5 65536 bit Static CMOS RAM

IC UPD4364G-15L

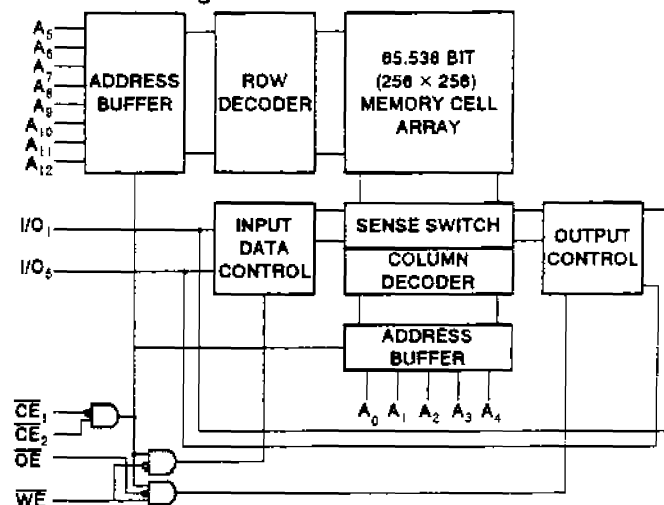
IC MB8464A-80

IC MB8464A-10LL

Top view & Pin Layout



Block Diagram



Operation Mode

\overline{CE}_1	\overline{CE}_2	\overline{OE}	WE	MODE	OUTPUT STATE	POWER SUPPLY CURRENT
H	x	x	x	Non-select (Power down)	High impedance	I_{SB}
x	L	x	x			
L	H	H	H	Output disable		I_{CCA}
L	H	L	H	Read	D_{OUT}	
L	H	x	L	Write	D_{IN}	

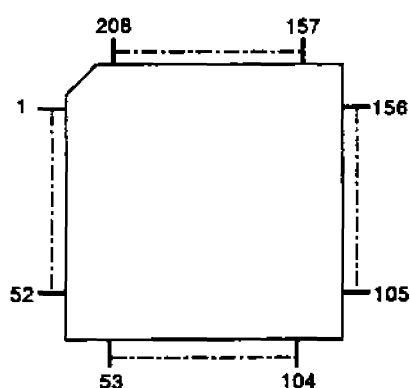
IC6 CUSTOM IC

IC CUSTOM CHIP SGE FC1004
315-5487-R

IC CUSTOM CHIP SGE FC1004
837-5487-01R

IC CUSTOM CHIP SGE FC1004
315-5487-01R

Top View & Pin Layout



Description

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	SD0	I	Dual port RAM interface signals.	5	SD4	I	Dual port RAM interface signals.
2	SD1			6	SD5		
3	SD2			7	SD6		
4	SD3			8	SD7		

Pin No.	Name	I/O	Function	
9	SEI	O	Dual port RAM interface signals.	
10	SE0			
11	SC			
12	RASI			
13	CASI			
14	WEI			
15	WE0			
16	OEI	I/O	Dual port RAM interface signals.	
17	RD0			
18	RD1			
19	RD2			
20	RD3			
21	VSS	—	GND	
22	RD4	I/O	Dual port RAM interface signals.	
23	RD5			
24	RD6			
25	RD7			
26	AD0			
27	AD1			
28	AD2			
29	AD3			
30	AD4			
31	AD5			
32	AD6			
33	AD7			
34	VIDEO AVSS	—	VIDEO+PSG	
35	R (ANALOG)	O		
36	G (ANALOG)			
37	B (ANALOG)			
38	VIDEO AVDD	—		
39	YS	O		
40	SPA/B	I/O		
41	VS $\overline{\text{YNC}}$	O		
42	CS $\overline{\text{YNC}}$	I/O	VIDEO+PSG	
43	HS $\overline{\text{YNC}}$	I/O		
44	VDD	—	Power supply.	
45	M3	I	68000 interface signals.	
46	NTSC			
47	VPA			
48	HALT	O		
49	RESET			
50	FC0	I		
51	FC1			
52	MREQ	I/O	Z80 interface signals.	
53	VSS	—	GND	
54	AUSS	—	FM	
55	MOR	O		
56	MOL	—		
57	SOUND	—		
58	SOUND	I/O	Use this pin set to open certainly.	

Pin No.	Name	I/O	Function
59	ZRES	I/O	Z80 interface signals.
60	ZBAK	I	Z80 interface signals.
61	NMI	O	
62	ZBR	I/O	
63	WAIT		
64	EOE		
65	NOE	O	P-SRAM interface.
66	ZRAM	O	SRAM interface.
67	REF		
68	CAS2	O	
69	RAS2		
70	ASEL		
71	ROM		
72	FDC		
73	FDWR		
74	CEO		
75	TIME		
76	CART	I	
77	IA14	O	
78	WRES	I	
79	DISK	I/O	
80	VDD	—	Power supply.
81	TEST0	I/O	Test signal. (Set to “0” certainly.)
82	TEST1	I	Test signals. (These pins set to all open.)
83	TEST2		
84	TEST3		
85	PC0	I/O	Joy pad interface.
86	PC1		
87	PC2		
88	PC3		
89	PC4		
90	PC5		
91	PC6		
92	VSS	—	GND
93	PB0	I/O	Joy pad Interface.
94	PB1		
95	PB2		
96	PB3		
97	PB4		
98	PB5		
99	PB6		
100	PA0		
101	PA1		
102	PA2		
103	PA3	I/O	
104	PA4		
105	PA5		
106	PA6		
107	JAP		
108	FRES		

Pin No.	Name	I/O	Function
109	ZV	I/O	Use this pin set to open certainly.
110	VZ		
111	IO	I/O	Z80 address bus.
112	ZA0		
113	ZA1		
114	ZA2		
115	ZA3		
116	ZA4		
117	ZA5		
118	ZA6		
119	ZA7		
120	ZA8		
121	ZA9		
122	ZA10		
123	ZA11		
124	ZA12		
125	ZA13		
126	ZA14		
127	ZA15		
128	\overline{SRES}	I	
129	SEL1		
130	CLK	I/O	68000 interface signals.
131	SBCR	O	VIDEO+PSG
132	ZCLK	I/O	Z80 interface signals.
133	VSS	—	GND
134	MCLK	I	
135	EDCLK	I/O	
136	VDD	—	Power supply.
137	VD0	I/O	68000 data bus.
138	VD1		
139	VD2		
140	VD3		
141	VD4		
142	VD5		
143	VD6		
144	VD7		
145	VD8		
146	VD9		
147	VD10		
148	VD11		
149	VD12		
150	VD13		
151	VD14		
152	VD15		
153	VSS	—	GND
154	VA1	I/O	68000 address bus.
155	VA2		
156	VA3		
157	VA4		
158	VA5		

Pin No.	Name	I/O	Function
159	VA6	I/O	68000 address bus.
160	VA7		
161	VA8		
162	VA9		
163	VA10		
164	VA11		
165	VA12		
166	VA13		
167	VA14		
168	VA15		
169	VA16		
170	VA17		
171	VA18		
172	VA19		
173	VA20		
174	VA21		
175	VA22		
176	VA23		
177	SOUND	—	VIDEO+PSG
178	PSG (ANALOG)	O	
179	SOUND AVSS	—	
180	VSS	—	GND
181	$\overline{\text{INT}}$	O	Z80 interface signals.
182	$\overline{\text{BR}}$	O	68000 interface signals.
183	$\overline{\text{BGACK}}$	I/O	
184	$\overline{\text{BG}}$	I	
185	$\overline{\text{IPL1}}$	O	
186	$\overline{\text{IPL2}}$	I	Z80 interface signals.
187	$\overline{\text{TORQ}}$	O	
188	$\overline{\text{ZRD}}$	I	
189	$\overline{\text{ZWR}}$	I/O	
190	$\overline{\text{MI}}$	I	68000 interface signals.
191	$\overline{\text{AS}}$	I/O	
192	$\overline{\text{UDS}}$		
193	$\overline{\text{LDS}}$		
194	R/W		
195	$\overline{\text{DTAK}}$		
196	$\overline{\text{UWR}}$	O	P-SRAM interface.
197	$\overline{\text{LWR}}$	I/O	
198	$\overline{\text{CASO}}$	I/O	
199	$\overline{\text{RASO}}$	O	P-SRAM interface.
200	ZD0	I/O	Z80 data bus.
201	ZD1		
202	ZD2		
203	ZD3		
204	ZD4		
205	ZD5		
206	ZD6		
207	ZD7		
208	VDD	—	Power supply.

IC7/8 65536 Word \times 4bit Dynamic RAM

IC M5M4C264L-12

IC M5M4C264L-15

IC UPD41264V-12

IC MB81461-12

IC HM53461ZP-12

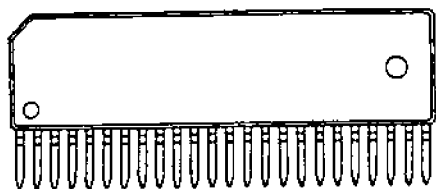
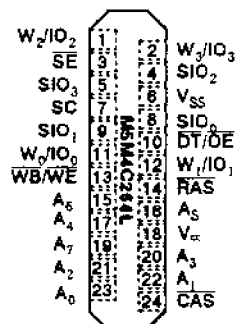
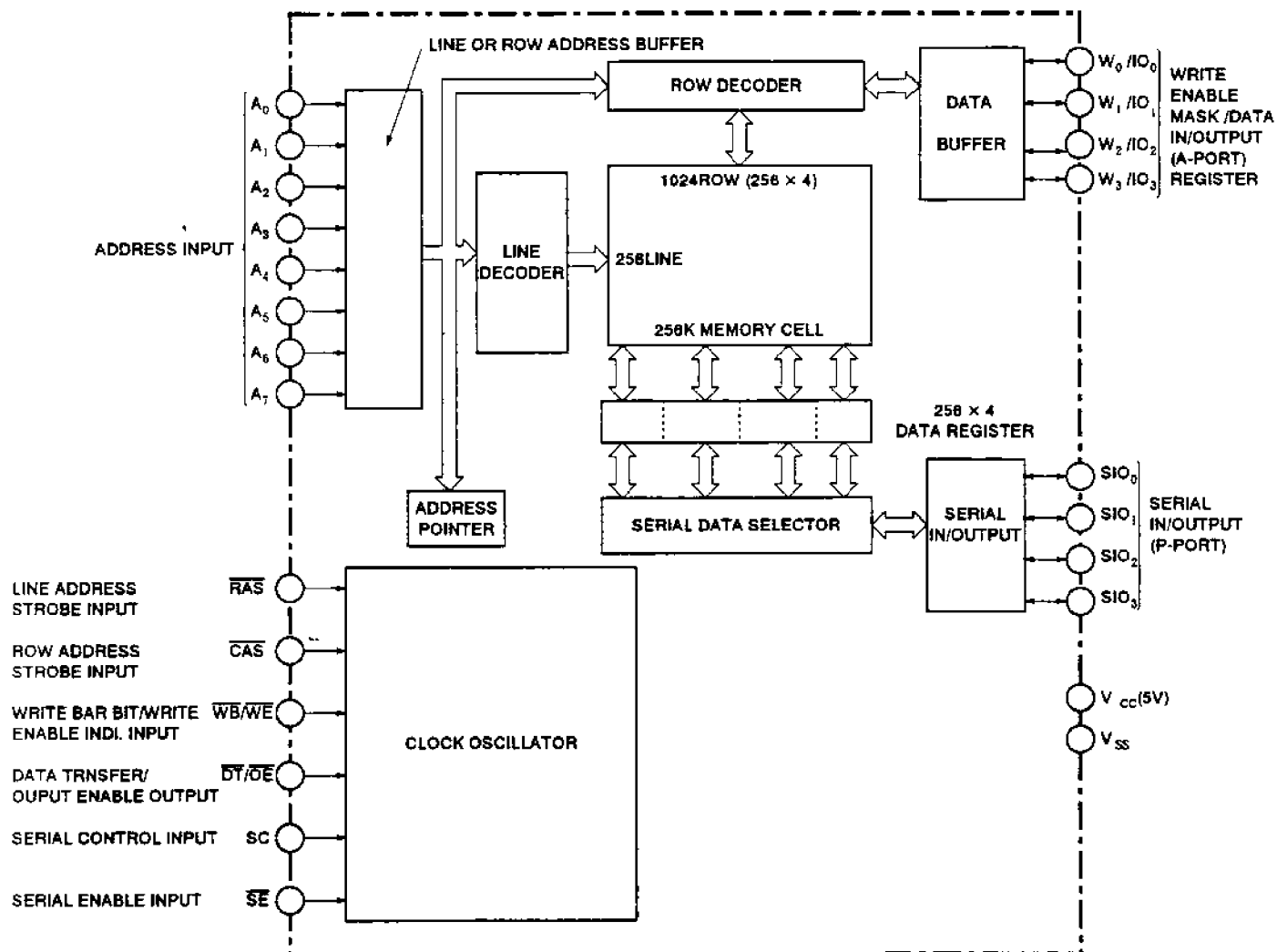
IC TMS4461-12SDL

IC V53C261Z10

IC KM424C64Z-10

IC MSM51C262-10ZS

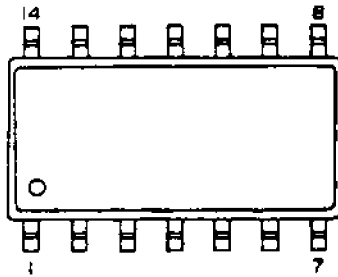
IC KM424C64Z-12

■ Outside View

■ Pin Layout

■ Block Diagram


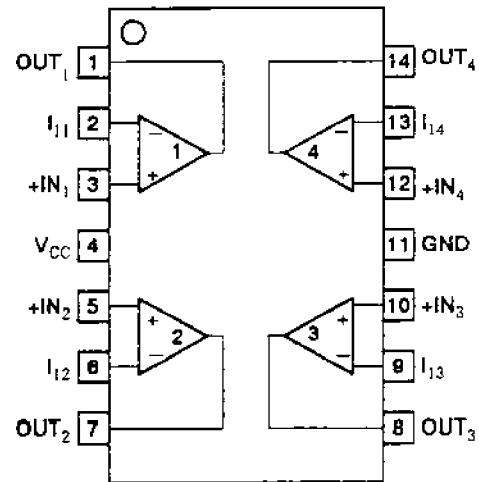
IC9/10 Quad Operational Amplifier

IC LM324

■ Top View



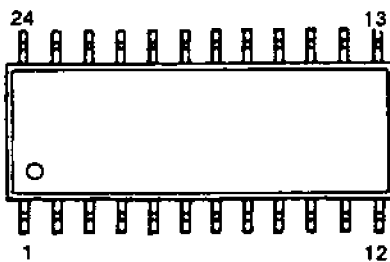
■ Pin Layout



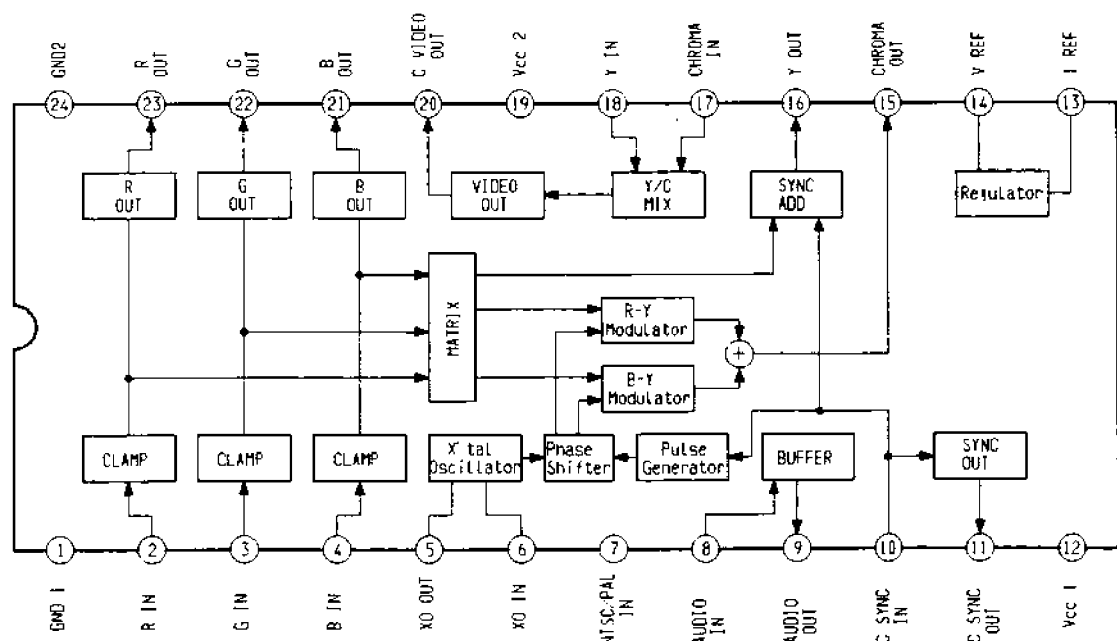
IC11 RGB Encoder

IC CXA1145M-T6

■ Top View



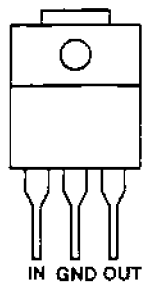
■ Pin Layout



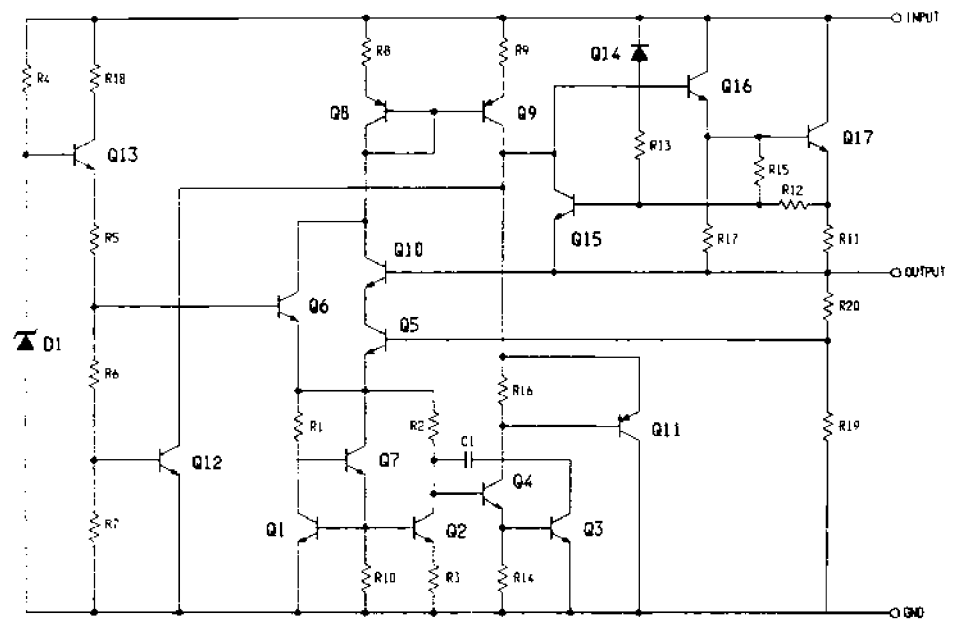
IC12

IC UPC7805HF

■ Top View



■ Block Diagram



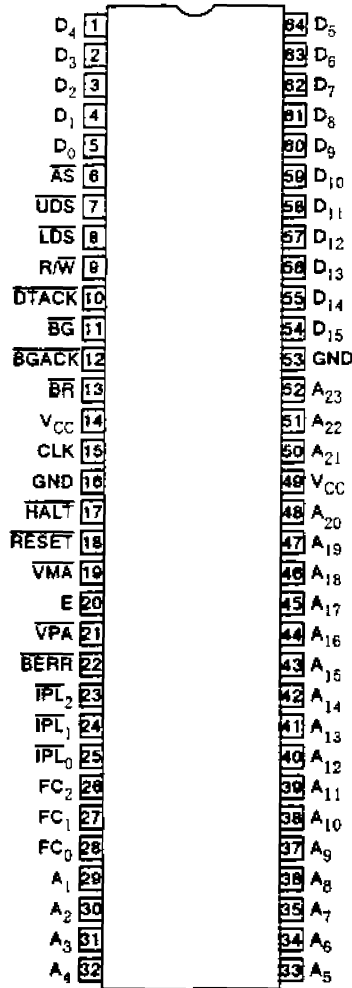
PARTS SPECIFICATIONS

IC1 16/32-bit Microprocessor

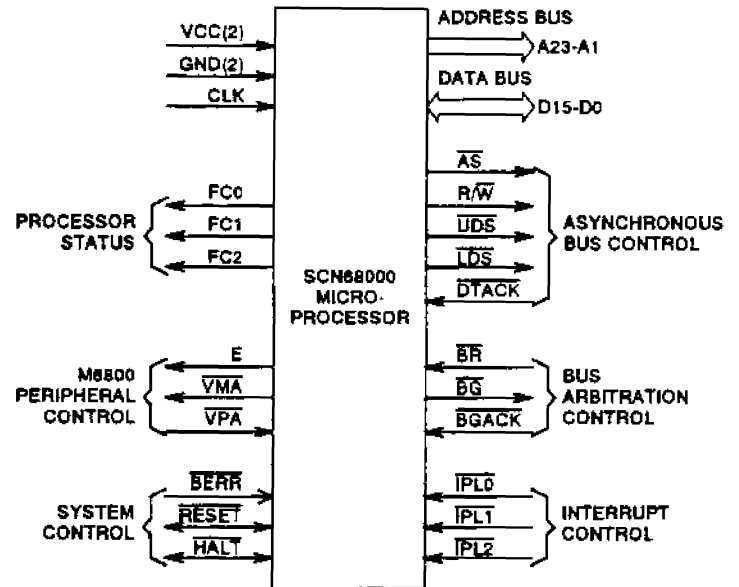
IC SCN68000C8N64

IC MC68000P8

■ Top View & Pin Layout



■ Signal Description



■ Description

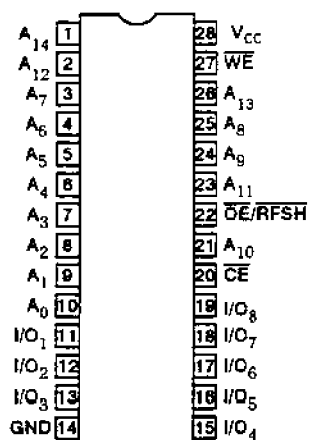
No.	Pin Name	I/O	Function	No.	Pin Name	I/O	Function	No.	Pin Name	I/O	Function
1	D ₄	I/O	Data bus	22	\overline{BERR}	I	Bus error	44	A ₁₆	O	Address bus
2	D ₃			23	\overline{IPL}_2	I	Interrupt control	45	A ₁₇		
3	D ₂			24	\overline{IPL}_1			46	A ₁₈		
4	D ₁			25	\overline{IPL}_0			47	A ₁₉		
5	D ₀			26	FC ₂	O	Processor status	48	A ₂₀		
6	\overline{AS}	O	Address strobe	27	FC ₁			49	V _{CC}	--	Power supply
7	\overline{UDS}	O	Upper data strobe	28	FC ₀			50	A ₂₁	O	Address bus
8	\overline{LDS}	O	Lower data strobe	29	A ₁	O	Address bus	51	A ₂₂		
9	R/W	O	Read/write	30	A ₂			52	A ₂₃		
10	DTACK	I	Data transfer Acknowledge	31	A ₃			53	V _{SS}	--	GND
11	\overline{BG}	O	Bus grant	32	A ₄			54	D ₁₅	I/O	Data bus
12	\overline{BGACK}	I	Bus grant acknowledge	33	A ₅			55	D ₁₄		
13	\overline{BR}	I	Bus request	34	A ₆			56	D ₁₃		
14	V _{CC}	--	Power supply	35	A ₇			57	D ₁₂		
15	CLK	I	Clock	36	A ₈			58	D ₁₁		
16	V _{SS}	--	GND	37	A ₉			59	D ₁₀		
17	\overline{HALT}	I/O	Halt	38	A ₁₀			60	D ₉		
18	\overline{RESET}	I/O	Reset	39	A ₁₁			61	D ₈		
19	VMA	O	Valid memory address	40	A ₁₂			62	D ₇		
20	E	O	Enable	41	A ₁₃			63	D ₆		
21	VPA	I/O	Valid peripheral address	42	A ₁₄			64	D ₅		
				43	A ₁₅						

IC2/3 32768 Word × 8bit CMOS Pseudo-Static RAM

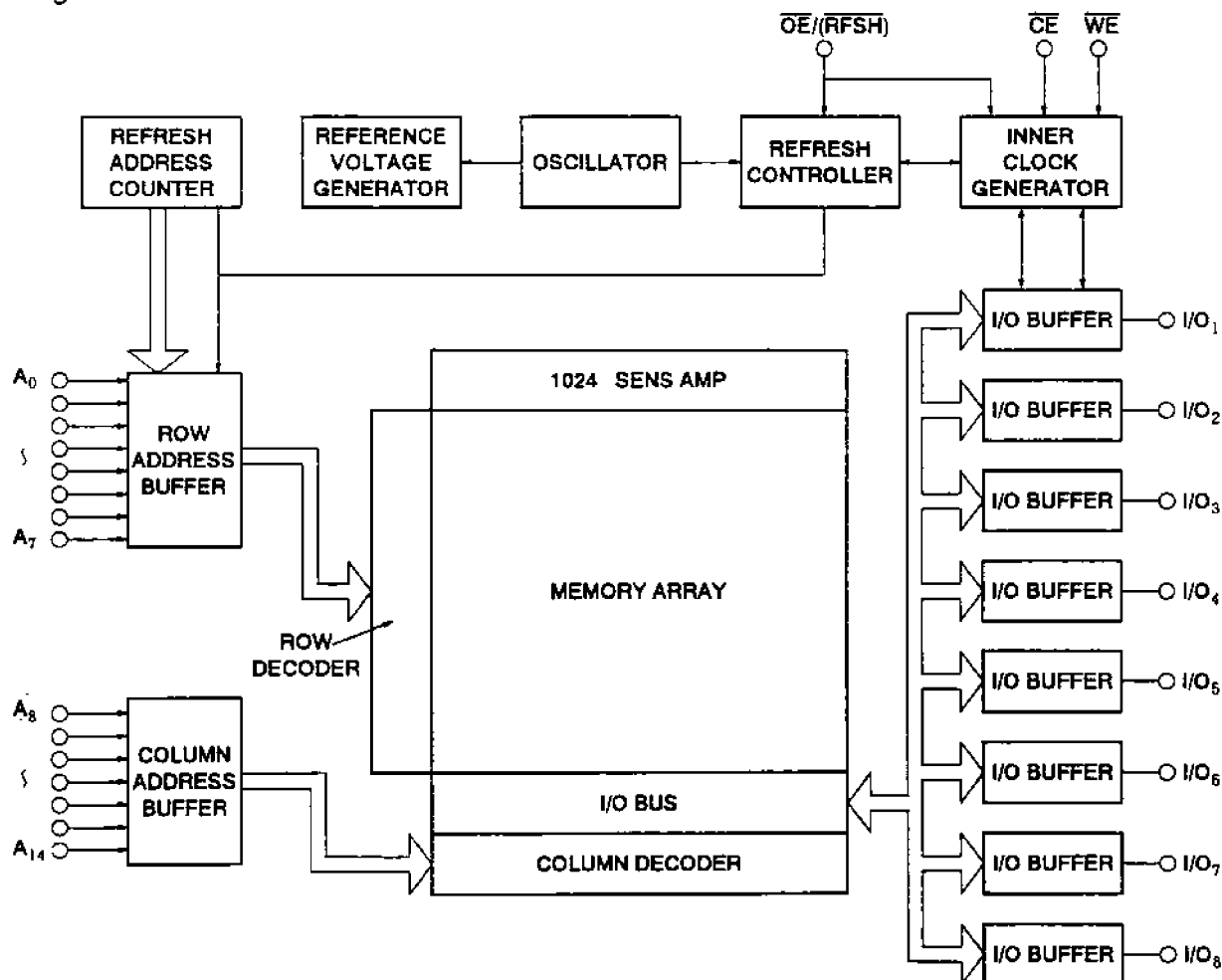
IC HM65256BSP-15

IC UPD42832C-15

IC TC51832-12

■ Top View & Pin Layout

■ Pin Name

Pin Name	Function
A0~A14	Address input
WE	Write enable input
$\overline{\text{OE/RFSH}}$	Output enable input/refresh input
CE	Chip enable input
I/O1~I/O8	Data input/output
V _{CC}	Power supply
GND	Ground

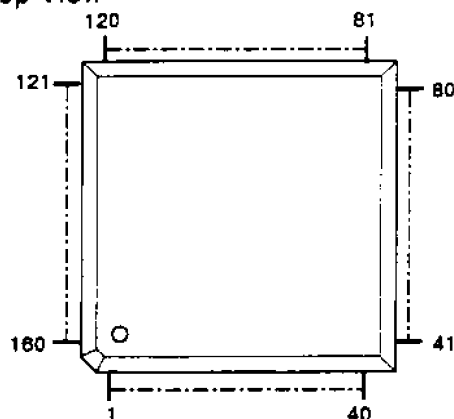
■ Block Diagram


IC4

IC CUSTOM CHIP UPD92271

Parts No. : 315-5433

■ Top View



■ Pin Name

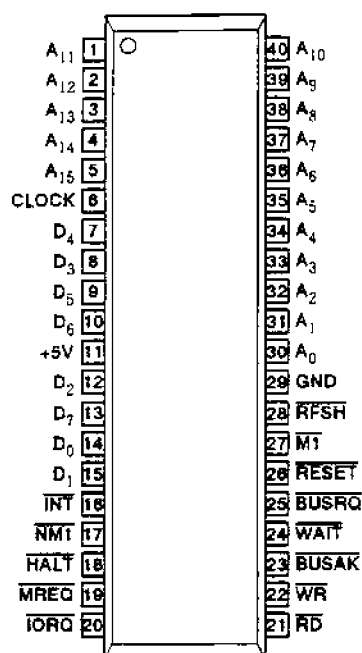
No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
1	VDD	41	GND	81	VDD	121	GND
2	MCLK	42	GND	82	A07	122	GND
3	CART	43	ZA4	83	A08	123	VCLK
4	ZRMM	44	ZA3	84	A09	124	XM3
5	XREF	45	ZA2	85	A10	125	XAS
6	XM1	46	ZA1	86	A11	126	LDS
7	ZRSS	47	ZA0	87	A12	127	UDS
8	XZBR	48	QA4	88	A13	128	RW0
9	WAI	49	QA6	89	A14	129	DTK
10	ZBAK	50	QA0	90	A15	130	BG
11	ZWW	51	QA1	91	A16	131	BGA
12	ZRR	52	QA2	92	A17	132	BR
13	IREQ	53	QA3	93	A18	133	HALT
14	MRQ	54	QA5	94	A19	134	VRES
15	XNMI	55	QB4	95	A20	135	XVPA
16	ZD1	56	QB6	96	A21	136	FC0
17	ZD0	57	QB0	97	A22	137	FC1
18	ZD7	58	QB1	98	A23	138	D00
19	GND	59	QB2	99	GND	139	D01
20	VDD	60	QB3	100	VDD	140	D02
21	GND	61	QB5	101	HL	141	D03
22	ZCLK	62	QC0	102	XFDW	142	D04
23	WRES	63	QC1	103	XFDC	143	D05
24	ZD2	64	QC2	104	XDIS	144	D06
25	ZD6	65	QC3	105	FRES	145	D07
26	ZD5	66	QC4	106	VDPM	146	D08
27	ZD3	67	QC5	107	XROM	147	D09
28	ZD4	68	QC6	108	ASEL	148	D10
29	ZAF	69	TST0	109	XTIM	149	D11
30	ZAE	70	TST1	110	RAS2	150	D12
31	ZAD	71	TST2	111	CAS2	151	D13
32	ZAC	72	XJAP	112	XOE0	152	D14
33	ZAB	73	A01	113	CAS0	153	D15
34	ZAA	74	A02	114	SRES	154	NTS
35	ZA9	75	A03	115	XCE0	155	HSYC
36	ZA8	76	A04	116	XLWR	156	SOUN
37	ZA7	77	A05	117	IA14	157	INTA
38	ZA6	78	A06	118	XNOE	158	EDCK
39	ZA5	79	GND	119	XEOE	159	GND
40	VDD	80	GND	120	VDD	160	GND

IC6 Z80A Central Processing Unit

IC Z80A

Parts No. : 315-0041

■ Top View & Pin Layout



■ Description

Pin	Pin Name	I/O	Function
30-40 1-5	A0-A15	3-STATE O	System address bus.
15-12 7-10	D0-D7	3-STATE I/O	System data bus.
6	CLOCK	I	Receives a +5V single-phase clock signal.
16	INT	I	Active "Low". If the input/output device issues a signal that requests an interrupt to the Z80 CPU and the interrupt enable flag is zero, this interrupt request is accepted at the end of the instruction that is currently in progress.
17	NMI	I	Active "Low". This is an interrupt request that has priority over INT and cannot be inhibited by the software. NMI is always accepted, and when the instruction that is currently in progress finishes, interrupt processing is started and the Z80 CPU automatically starts from address 0066H.
18	HALT	O	Active "Low". This indicated that the HALT instruction is being executed. Executes the NOP instruction internally and also refreshes memory. The halt state is released by RESET, NMI or INT (when enabled).
19	MREQ	3-STATE O	Active "Low". This indicated that the address bus outputs the effective memory address for memory read/write.
20	IORQ	3-STATE O	Active "Low". This indicates that the low-order 8 bits of the address bus output effective addresses of the input/output device for the read/write operation with this device. This is output together with MI during an interrupt response to indicate the response.
21	RD	3-STATE O	Active "Low". This indicates the timing with which data from the memory or input/output device is read.
22	WR	3-STATE O	Active "Low". This indicates that the effective data to be written to the memory or input/output device the address of which is specified is on the data bus.
23	BUSAK	O	When the bus request is acknowledged, this informs the bus master which outputs the bus request that the system bus can be controlled.
24	WAIT	I	Active "Low". Signal to inform the CPU that the memory or input/output device the address of which is specified is not ready to send data. The CPU is waiting when this signal is input.
25	BUSRQ	I	Active "Low". This has priority over NMI and is accepted at the end of the machine cycle that is currently in progress. This is set to "Low" when a bus master other than the CPU wants to control the system bus.
26	RESET	I	Active "Low". This resets the interrupt enable flag, interrupt vector register and memory refresh register of the program counter to set the interrupt mode to mode 0, thus initializing the Z80 CPU.
27	MI	O	Active "Low". This indicates that the machine cycle being executed is an OP code fetch cycle.
28	RFSH	O	Active "Low". This indicates that the address for refreshing the dynamic RAM is output to the low-order 7 bits of the address bus. MREQ also goes "Low" at this time.

IC7 65536 bit Static CMOS RAM

IC UPD4168C-20

IC UPD4168C-15

IC UPD4168C-15-SG

IC UPD4364C-15

IC UPD4364CX

IC MB8464A-15L

IC TMM2064-15

IC TMM2063-12

IC HM6264L-120

IC KM6264BL-12 DIP600

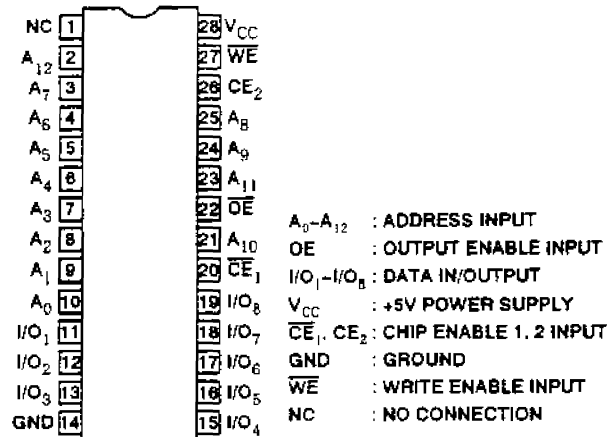
IC KM6264BLS-12L DIP300

IC HM6265L-90

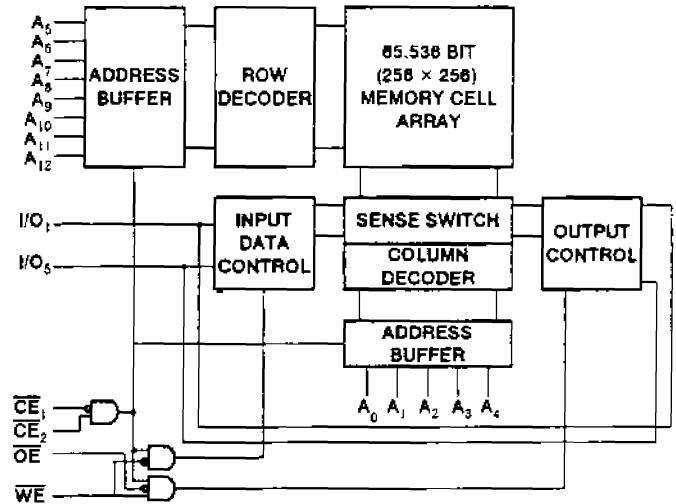
IC HY6264LP-15

IC KM4264L-15

Top View & Pin Layout



Block Diagram



Operation Mode

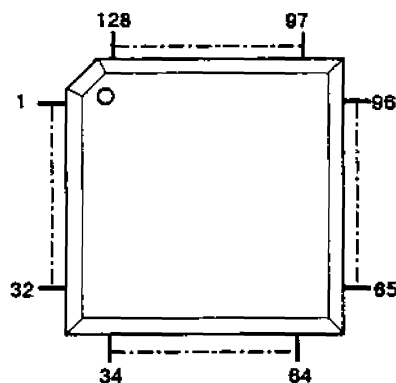
\overline{CE}_1	\overline{CE}_2	\overline{OE}	\overline{WE}	MODE	OUTPUT STATE	POWER SUPPLY CURRENT
H	x	x	x	Non-select (Power down)	High impedance	I_{SS}
x	L	x	x			
L	H	H	H	Output disable		I_{CCA}
L	H	L	H	Read	D_{OUT}	
L	H	x	L	Write	D_{IN}	

IC8 CUSTOM IC

IC CUSTOM CHIP YM7101

Parts No. : 315-5313

Top View & Pin Layout



Description

No.	Pin Name	I/O	Function	No.	Pin Name	I/O	Function
1	SD ₀	I	VRAM serial data bus.	50	SBCR	O	Sub carrier output (4.47/3.58MHz clock)
2	SD ₁			51	CLK ₀	O	Z80 CPU clock (3.58MHz)
3	SD ₂			52	MCK	I	Master clock input (53.7MHz).
4	SD ₃			53	EDCK	I/O	Dot clock input/output (13.4/10.7MHz).
5	SD ₄			54	VDD	I	Digital VDD.
6	SD ₅			55	CD ₀	I/O	CPU data bus.
7	SD ₆			56	CD ₁		
8	SD ₈			57	CD ₂		
9	SE ₁	O	VRAM strobe/control.	58	CD ₃		
10	SE ₀			59	CD ₄		
11	SC			60	CD ₅		
12	RAS ₁			61	CD ₆		
13	CAS ₁			62	CD ₇		
14	WE ₁			63	CD ₈		
15	WE ₀			64	CD ₉		
16	OE ₁			65	CD ₁₀		
17	GND	—	GND	66	CD ₁₁		
18	RD ₀	I/O	VRAM data bus.	67	CD ₁₂		
19	RD ₁			68	CD ₁₃		
20	RD ₂			69	CD ₁₄		
21	RD ₃			70	CD ₁₅		
22	RD ₄			71	CA ₀	I/O	CPU address bus.
23	RD ₅			72	CA ₁		
24	RD ₆			73	CA ₂		
25	RD ₇			74	CA ₃		
26	AGC	—	RGB analog GND.	75	CA ₄		
27	R (ANLONG)	O	Linear RGB output.	76	CA ₅		
28	G (ANLONG)			77	CA ₆		
29	B (ANLONG)			78	CA ₇		
30	AVC	—	RGB analog VDD.	79	CA ₈		
31	AD ₀	I/O	VRAM address/data bus.	80	CA ₉		
32	AD ₁			81	CA ₁₀		
33	AD ₂			82	CA ₁₁		
34	AD ₃			83	CA ₁₂		
35	AD ₄			84	CA ₁₃		
36	AD ₅			85	CA ₁₄		
37	AD ₆			86	CA ₁₅		
38	AD ₇			87	CA ₁₆		
39	YS	O	Transparent output.	88	CA ₁₇		
40	SPA/B	I/O	Sprite timing I/O.	89	CA ₁₈		
41	VSYNC	O	CRT Vsync out/dot clock out.	90	CA ₁₉		
42	CSYNC	I/O	VIDEO+PSG	91	CA ₂₀		
43	HSYNC	I/O	CRT HSYNC input/output	92	CA ₂₁		
44	HL	I	Light pen detect	93	CA ₂₂		
45	SEL ₀	I	CPU select (68000/Z80)	94	AYS	I	Sound analog GND.
46	PAL	I	CRT select (NTSC/PAL)	95	SOUND	O	Sound analog output.
47	RESET	I	Initial reset input.	96	AGS	I	Sound analog VDD.
48	SEL ₁	I	68000 CPU clock (CLK1) I/O control.	97	GND	I	Digital GND.
49	CLK ₁	I/O	68000 CPU clock (7.67MHz)	98	INT	O	Z80 interface.

No.	Pin Name	I/O	Function
99	$\overline{\text{BR}}$	O	68000 interface.
100	$\overline{\text{BGAK}}$	I/O	
101	$\overline{\text{BG}}$	I	
102	$\overline{\text{MREQ}}$	I	Z80 interface.
103	$\overline{\text{INTAK}}$	I	68000 interface.
104	$\overline{\text{IPL}}_1$	O	
105	$\overline{\text{IPL}}_2$		
106	$\overline{\text{IORQ}}$	I	Z80 interface.
107	$\overline{\text{RD}}$		
108	$\overline{\text{WR}}$		
109	$\overline{\text{MI}}$		
110	$\overline{\text{AS}}$	I	68000 interface.
111	$\overline{\text{UDS}}$		
112	$\overline{\text{LDS}}$		
113	R/W		

No.	Pin Name	I/O	Function
114	$\overline{\text{DTAK}}$	I/O	68000 interface.
115	$\overline{\text{UWR}}$	O	Work RAM strobe control.
116	$\overline{\text{LWR}}$		
117	$\overline{\text{OE0}}$		
118	CAS_0		
119	RAS_0	O	Work RAM (DRAM) address/color code output.
120	RA_0		
121	RA_1		
122	RA_2		
123	RA_3		
124	RA_4		
125	RA_5		
126	RA_6		
127	RA_7		
128	VDD	I	Digital VDD.

IC9/10 65536 Word \times 4bit Dynamic RAM

IC M5M4C264L-12

IC M5M4C264L-15

IC UPD41264V-12

IC MB81461-12

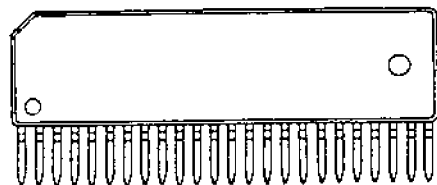
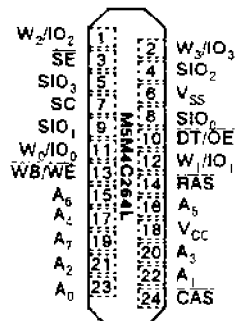
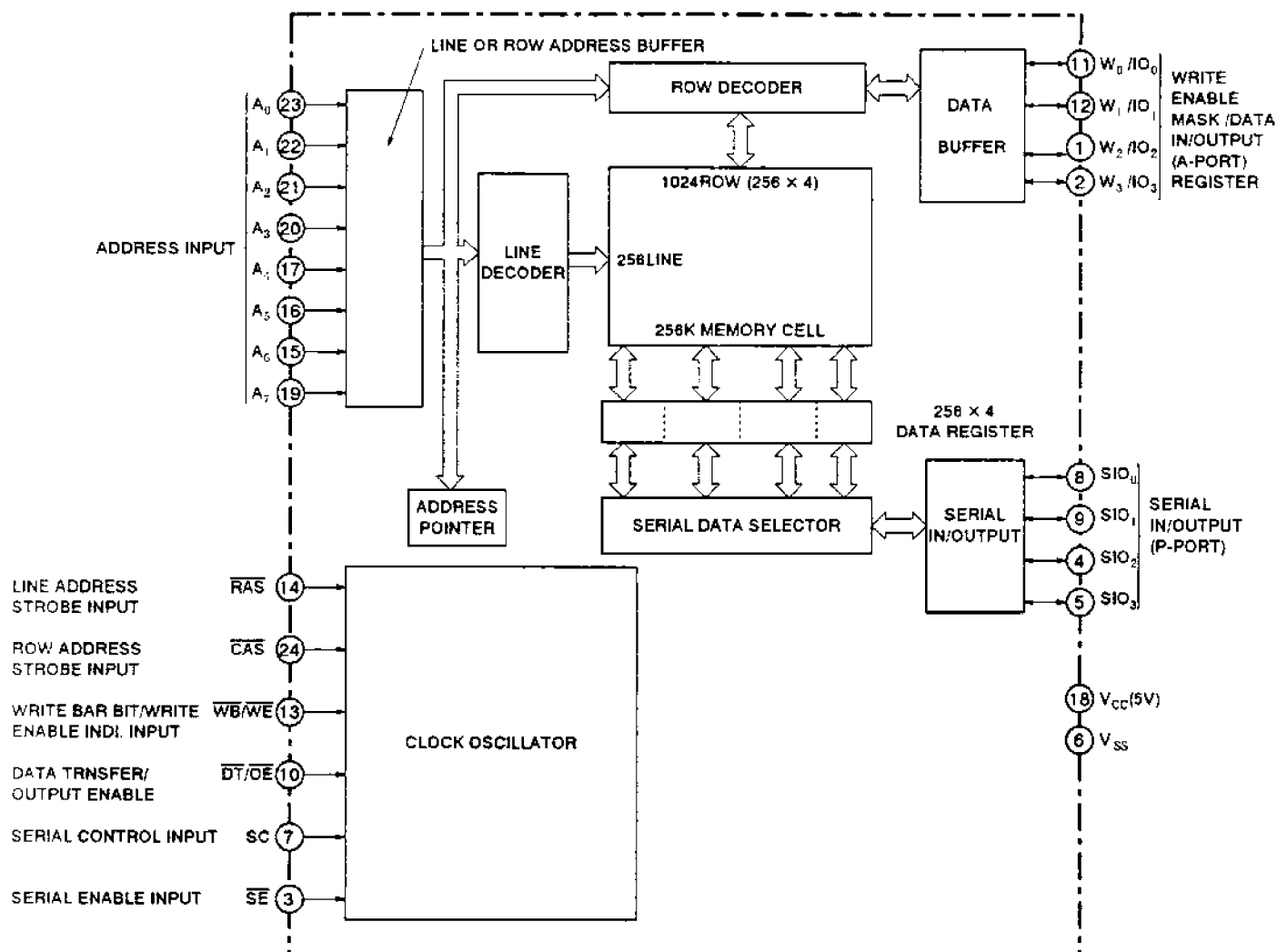
IC HM53461ZP-12

IC TMS4461-12SDL

IC V53C261Z10

IC KM424C64Z-10

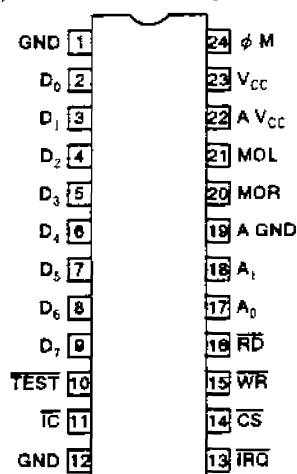
IC MSM51C262-10ZS

■ Outside View

■ Pin Layout

■ Block Diagram


IC11 FM Sound Source/DA Converter

IC YM2612

■ Top View & Pin Layout



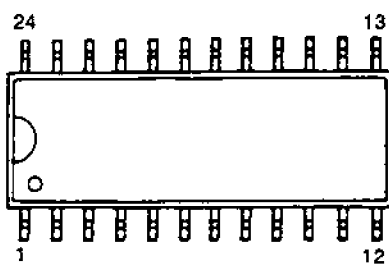
■ Description

No.	Pin Name	I/O	Function																																																						
1	GND	—	Ground pin.																																																						
2	D ₀	I/O	8-bit bidirectional data bus. Communicates data with the processor.																																																						
3	D ₁																																																								
4	D ₂																																																								
5	D ₃																																																								
6	D ₄																																																								
7	D ₅																																																								
8	D ₆																																																								
9	D ₇																																																								
10	TEST	I/O	Pin to test this LSI. Do not connect.																																																						
11	IC	I	Initializes the internal register.																																																						
12	GND	—	Ground pin.																																																						
13	IRQ	O	Interrupt signal issued from the two timers. When the time programmed into the timer has elapsed, this goes low. Output with open drain.																																																						
14	CS	I	Control the D0 – D7 data bus. <table><tr><th>CS</th><th>RD</th><th>WR</th><th>A1</th><th>A0</th><th>Details</th></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Writes register addresses of timers, etc.</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td>Writes register addresses of channels 1-3.</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Writes register data of timers, etc.</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td>Writes register data of channels 1-3.</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Writes register addresses of channels 4-6.</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Writes register data of channels 4-6.</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Reads statuses.</td></tr><tr><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>D0 – D7 are set to high-impedance.</td></tr></table>	CS	RD	WR	A1	A0	Details	0	1	0	0	0	Writes register addresses of timers, etc.						Writes register addresses of channels 1-3.	0	1	0	0	1	Writes register data of timers, etc.						Writes register data of channels 1-3.	0	1	0	1	0	Writes register addresses of channels 4-6.	0	1	0	1	1	Writes register data of channels 4-6.	0	0	1	0	0	Reads statuses.	1	X	X	X	X	D0 – D7 are set to high-impedance.
CS	RD		WR	A1	A0	Details																																																			
0	1		0	0	0	Writes register addresses of timers, etc.																																																			
						Writes register addresses of channels 1-3.																																																			
0	1		0	0	1	Writes register data of timers, etc.																																																			
						Writes register data of channels 1-3.																																																			
0	1		0	1	0	Writes register addresses of channels 4-6.																																																			
0	1		0	1	1	Writes register data of channels 4-6.																																																			
0	0	1	0	0	Reads statuses.																																																				
1	X	X	X	X	D0 – D7 are set to high-impedance.																																																				
15	WR																																																								
16	RD																																																								
17	A ₀																																																								
18	A ₁																																																								
19	A GND	—	Ground pin.																																																						
20	MOR	O	Two-channel analog outputs. These are output with a source follower.																																																						
21	MOL																																																								
22	A V _{CC}	—	+5V power supply pins.																																																						
23																																																									
24	φ M V _{CC}	I	Master clock input.																																																						

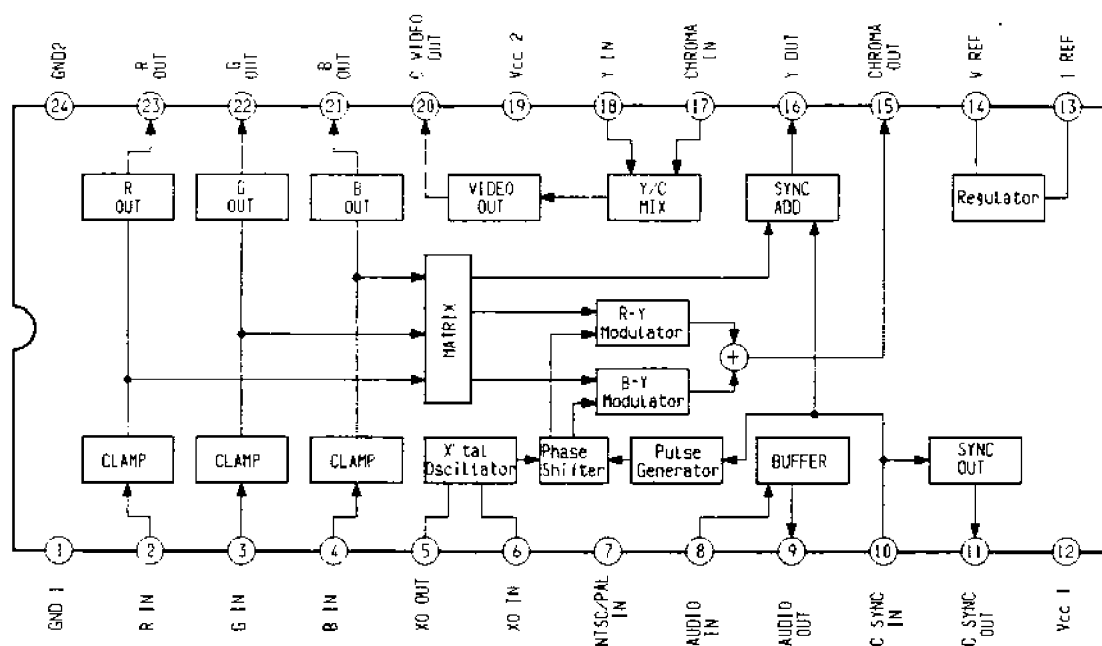
IC13 RGB Encoder

IC CXA1145P

Top View



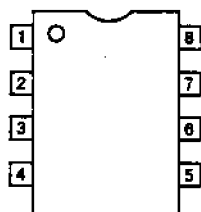
Pin Layout



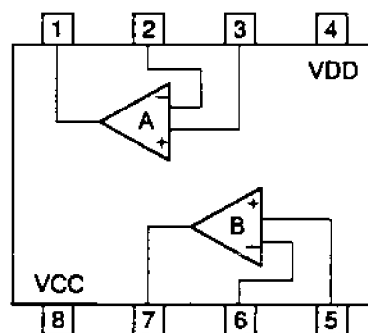
IC14 Dual Operational Amplifier

IC LM358

Top View



Pin Layout



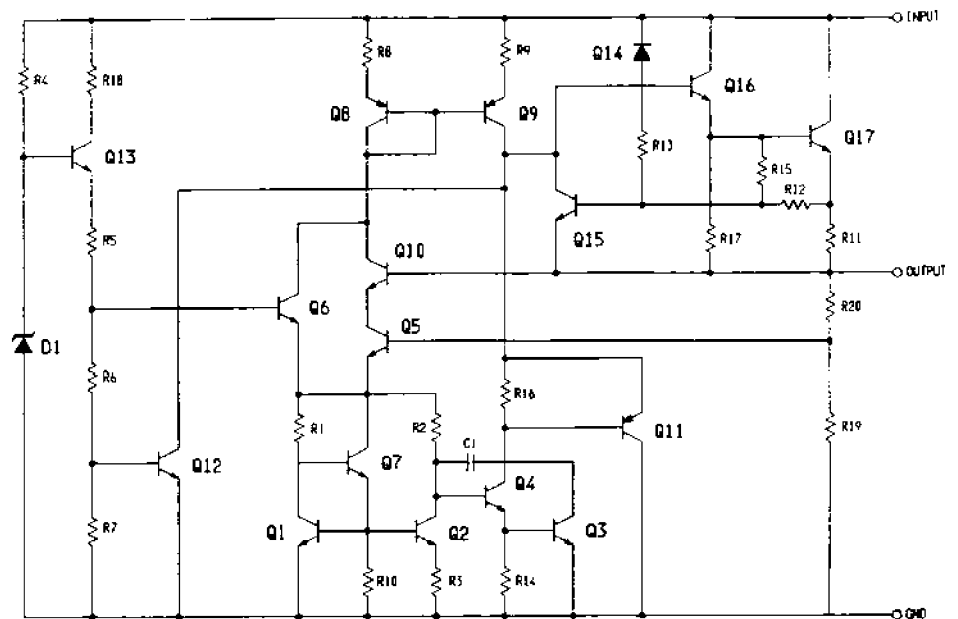
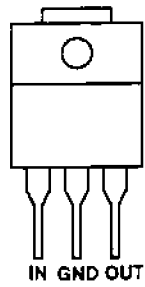
IC15,17 Three Terminal Regulator

IC MA7805UC

IC_MC7805CT

■ Top View

■ Block Diagram



PARTS SPECIFICATION

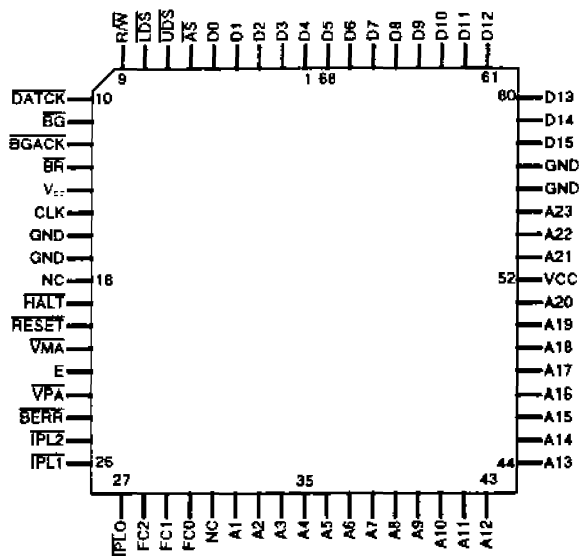
IC1 16/32-Bit Microprocessor

IC MC68HC000FN12

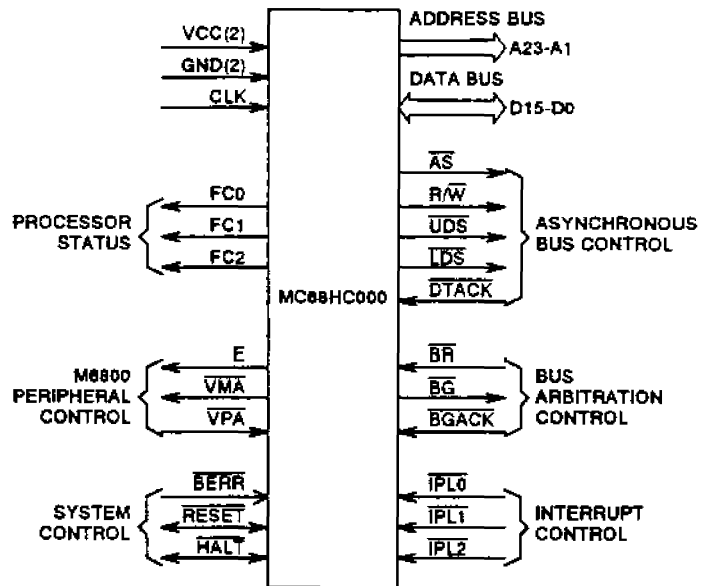
IC HD68HC000CP-12

IC TMP68HC000T-12

■ Top View & Pin Layout



■ Signal Description

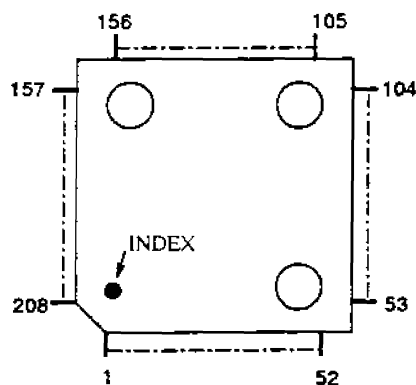


■ Description

No.	Pin Name	I/O	Function	No.	Pin Name	I/O	Function	No.	Pin Name	I/O	Function
1	D ₁	I/O	Data Bus	23	VPA	I	Valid Peripheral Address	46	A ₁₅	O	Address Bus
2	D ₂			24	BERR	I	Bus Error	47	A ₁₆		
3	D ₂			25	IPL ₂	I	Interrupt Control	48	A ₁₇		
4	D ₁			26	IPL ₁			49	A ₁₈		
5	D ₀			27	IPL ₀			50	A ₁₉		
6	AS	O	Address Strobe	28	FC ₂	O	Processor Status	51	A ₂₀	O	Address Bus
7	UDS	O	Upper Data Strobe	29	FC ₁			52	V _{CC}	-	Power Supply
8	LDS	O	Lower Data Strobe	30	FC ₀			53	A ₂₁	O	Address Bus
9	R/W	O	Read/Write	31	N.C.	-		54	A ₂₂		
10	DTACK	I	Data Transfer Acknowledge	32	A ₁	O	Address Bus	55	A ₂₃		
11	BG	O	Bus Grant	33	A ₂			56	V _{SS}	-	GND
12	BGACK	I	Bus Grant Acknowledge	34	A ₃			57	V _{SS}	-	GND
13	BR	I	Bus Request	35	A ₄			58	D ₁₅	I/O	Data Bus
14	V _{CC}	-	Power Supply	36	A ₅			59	D ₁₄		
15	CLK	I	Clock	37	A ₆			60	D ₁₃		
16	V _{SS}	-	GND	38	A ₇			61	D ₁₂		
17	V _{SS}	-	GND	39	A ₈			62	D ₁₁		
18	NC	-	Not Connected	40	A ₉			63	D ₁₀		
19	HALT	I/O	Halt	41	A ₁₀			64	D ₉		
20	RES	I/O	Reset	42	A ₁₁			65	D ₈		
21	VMA	O	Valid Memory Address	43	A ₁₂			66	D ₇		
22	E	O	Enable	44	A ₁₃			67	D ₆		
				45	A ₁₄			68	D ₅		

IC2 CUSTOM CHIP MCE2

Parts No. : 315-5548

■ Top View**■ Description**

No.	I/O	Pin Name
1	O	OCK25
2	O	OBRAM
3	-	V _{SS}
4	I	OXBROM
5	I	IROM
6	I	ICASO
7	I	ILWR
8	I	IUWR
9	I	IASSEL
10	-	V _{DD}
11	I	IRAS2
12	I	ICAS2
13	I	IFDC
14	I	IFRES
15	-	V _{SS}
16	O	OERES
17	I/O	BEAD0
18	I/O	BEAD1
19	I/O	BEAD2
20	I/O	BEAD3
21	I/O	BEAD4
22	I/O	BEAD5
23	I/O	BEAD6
24	I/O	BEAD7
25	I/O	BED8
26	-	V _{SS}
27	-	V _{DD}
28	I/O	BED9
29	I/O	BED10
30	I/O	BED11
31	I/O	BED12
32	I/O	BED13
33	I/O	BED14
34	I/O	BED15
35	O	OERAS
36	O	OECAS
37	O	OEOE
38	-	V _{SS}
39	O	OEWEE
40	O	OORAS
41	O	OOCAS
42	O	OÖOE

No.	I/O	Pin Name
43	-	V _{DD}
44	O	OÖWE
45	I/O	BOAD0
46	I/O	BOAD1
47	I/O	BOAD2
48	I/O	BOAD3
49	I/O	BOAD4
50	-	V _{SS}
51	I/O	BOAD5
52	I/O	BOAD6
53	I/O	BOAD7
54	I/O	BOD8
55	I/O	BOD9
56	I/O	BOD10
57	I/O	BOD11
58	I/O	BOD12
59	I/O	BOD13
60	-	V _{SS}
61	-	V _{DD}
62	I/O	BOD14
63	I/O	BOD15
64	O	OEDR
65	O	OLEDG
66	O	OLATCH
67	O	OSHFT
68	O	OATT
69	O	ODTM
70	I	IWFCK
71	I	ISCOR
72	-	V _{SS}
73	I	ISBSO
74	O	OEXCK
75	I	ILRCK
76	I	IDATA
77	I	IC2PO
78	I/O	BDB3
79	-	V _{DD}
80	I/O	BDB2
81	I/O	BDB1
82	I/O	BDB0
83	O	OHOCK
84	I	ICK50

No.	I/O	Pin Name
85	-	V _{SS}
86	I	IIRQ
87	I	IDXM
88	I	ICDCK
89	O	OXPCM
90	I	IDTEN
91	I	IWAIT
92	O	OHRD
93	I	IINT
94	O	OCDC
95	O	OPROE
96	-	V _{SS}
97	-	V _{DD}
98	O	OC2LR
99	I	IA19
100	I	IA18
101	I	IA17
102	I	IA16
103	I	IA15
104	I	IA14
105	I/O	BA13
106	I/O	BA12
107	-	V _{SS}
108	I/O	BA11
109	I/O	BA10
110	I/O	BA9
111	I/O	BA8
112	I/O	BA7
113	I/O	BA6
114	-	V _{DD}
115	I/O	BA5
116	I/O	BA4
117	I/O	BA3
118	I/O	BA2
119	-	V _{SS}
120	I/O	BA1
121	I	IFC0
122	I	IFC1
123	O	OIPL0
124	O	OIPL1
125	O	OIPL2
126	O	OVPA
127	O	ORESET
128	O	OHALT
129	O	OCLK
130	-	V _{SS}
131	-	V _{DD}
132	O	ODTACK
133	I	IRXW
134	I	IXLDS
135	I	IXUDS
136	I	IXAS
137	I/O	BD0
138	I/O	BD1
139	I/O	BD2
140	I/O	BD3
141	I/O	BD4
142	-	V _{SS}
143	I/O	BD5
144	I/O	BD6
145	I/O	BD7
146	I/O	BD8

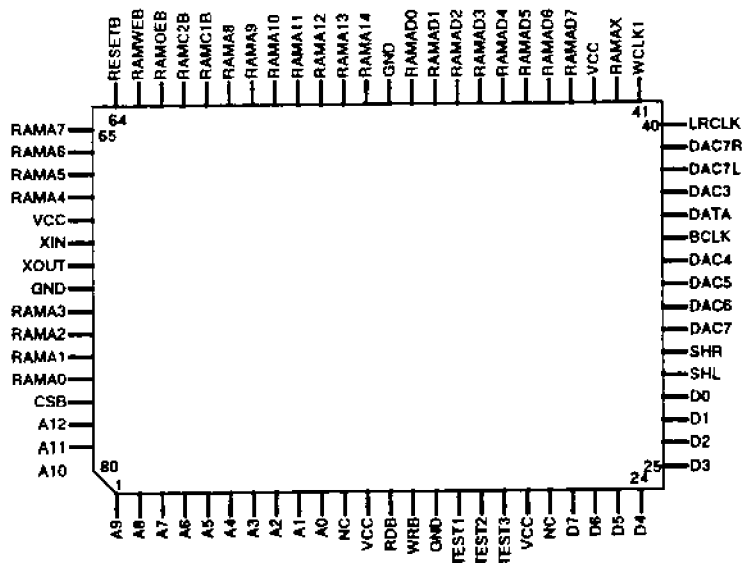
No.	I/O	Pin Name
147	-	V _{DD}
148	I/O	BD9
149	I/O	BD10
150	I/O	BD11
151	I/O	BD12
152	I/O	BD13
153	I/O	BD14
154	-	V _{SS}
155	I/O	BD15
156	I/O	BPRA0
157	I/O	BPRA1
158	I/O	BPRA2
159	I/O	BPRA3
160	I/O	BPRA4
161	I/O	BPRA5
162	I/O	BPRA6
163	I/O	BPRA7
164	-	V _{SS}
165	-	V _{DD}
166	I/O	BPRA8
167	O	OPRRAS
168	O	OPRCAS
169	O	OPRUWE
170	O	OPRLWE
171	I/O	IVA1
172	I/O	IVA2
173	I/O	IVA3
174	I/O	IVA4
175	I/O	IVA5
176	-	V _{SS}
177	I/O	IVA6
178	I/O	IVA7
179	I/O	IVA8
180	I/O	IVA9
181	I/O	IVA10
182	I/O	IVA11
183	-	V _{DD}
184	I/O	IVA12
185	I/O	IVA13
186	I/O	IVA14
187	I/O	IVA15
188	I/O	IVA16
189	-	V _{SS}
190	I	IVA17
191	I/O	BVD0
192	I/O	BVD1
193	I/O	BVD2
194	I/O	BVD3
195	I/O	BVD4
196	I/O	BVD5
197	I/O	BVD6
198	I/O	BVD7
199	I/O	BVD8
200	-	V _{SS}
201	-	V _{DD}
202	I/O	BVD9
203	I/O	BVD10
204	I/O	BVD11
205	I/O	BVD12
206	I/O	BVD13
207	I/O	BVD14
208	I/O	BVD15

IC3 PCM Sound Source

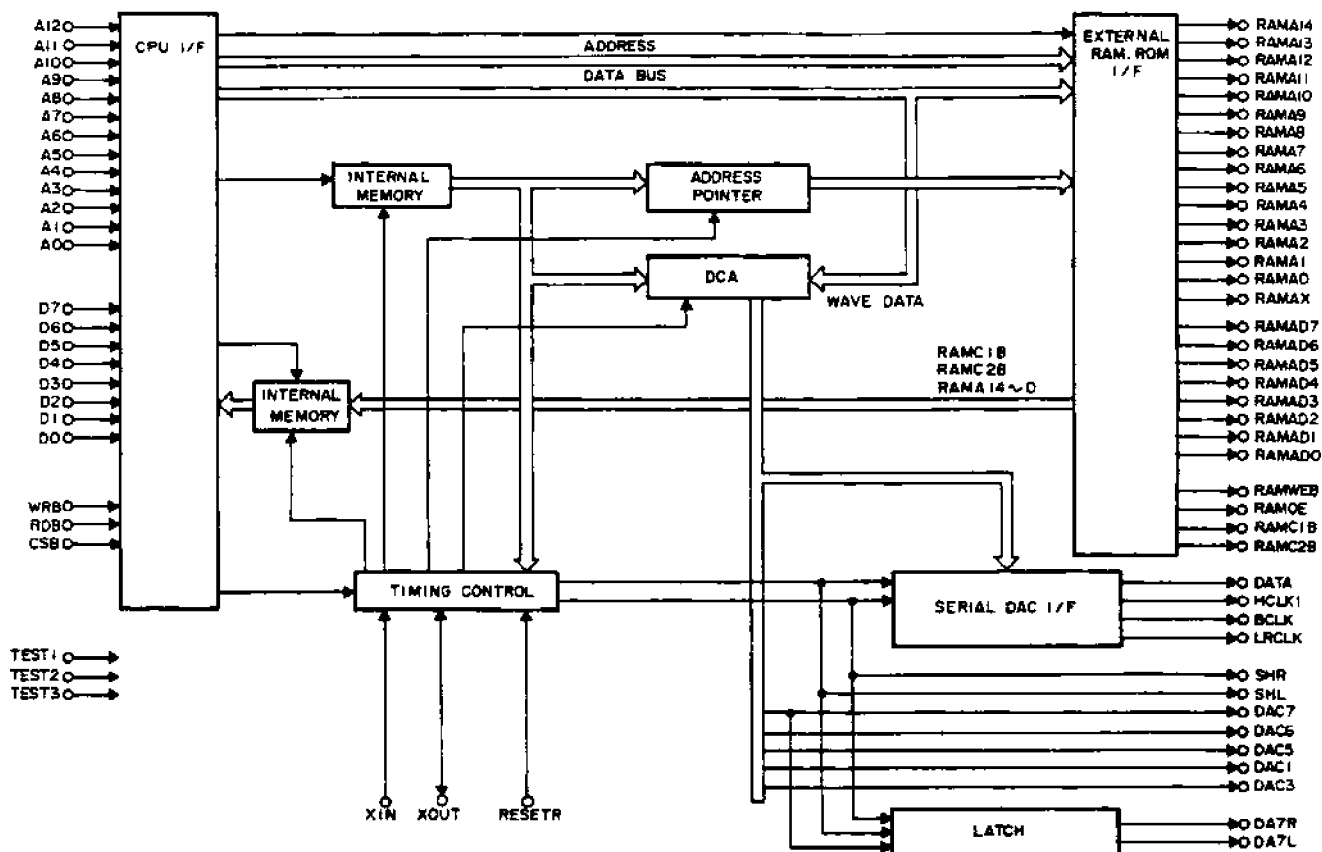
IC RF5C164A

Parts No. : 315-5476A

■ Top View & Pin Layout



■ Block Diagram



■ Description (IC3)

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
78	A12	I	Address signals from μ P.	75	RAMA1	O	Low address signals of the SRAM & MROM.
79	A11			76	RAMA0		
80	A10			42	RAMAX	O	LSB address signal of the MROM.
1	A9			61	RAMC2B	O	High order 32k byte SRAM & MROM select signal.
2	A8			60	RAMC1B	O	Low order 32k byte SRAM & MROM select signal.
3	A7			63	RAMWEB	O	Signal to write data to the pseudo SRAM or SRAM.
4	A6			62	RAMOEB	O	Signal to read data from the pseudo SRAM, SRAM or MROM.
5	A5			31	DAC7	O	Multiplex signals of "R" and "L" data output to the parallel DAC.
6	A4			32	DAC6		
7	A3			33	DAC5		
8	A2			34	DAC4		
9	A1			37	DAC3		
10	A0			29	SHL	O	DAC7-3 "L" data sample/hold signal.
21	D7	I/O	Data bus signals with μ P.	30	SHR	O	DAC7-3 "R" data sample/hold signal.
22	D6			39	DAC7R	O	Signal obtained by sampling and holding the DAC7 output at SHR.
23	D5			38	DAC7L	O	Signal obtained by sampling and holding the DAC7 output at SHL.
24	D4			41	WCLK1	O	Word clock signal output to the serial DAC.
25	D3			40	LRCLK	O	LR clock signal output to the serial DAC.
26	D2			36	DATA	O	Digital audio data signal output to the serial DAC.
27	D1			35	BCLK	O	Bit clock signal output to the serial DAC.
28	D0			64	RESETB	I	Reset signal.
77	CSB	I	Chip select signal from μ P.	70	XIN	I	An external crystal oscillator is connected. A clock signal is input to XIN directly.
13	RDB	I	Read signal from μ P.	71	XOUT	O	
14	WRB	I	Write signal from μ P.	16	TEST1	I	Test signal inputs. Normally, fixed at "L". However, TEST2 is fixed at "H" when an MROM or SRAM is used.
44	RAMAD7	I/O	When connected to a pseudo SRAM, these pins provide multiplex signals of the low order address/data to the SRAM, and when connected to an MROM, these pins provide data input signal from the MROM. When connected to an SRAM, these pins also provide data bus signals to the SRAM.	17	TEST2		
45	RAMAD6			18	TEST3		
46	RAMAD5			12	VCC	-	Power supply pins.
47	RAMAD4			19			
48	RAMAD3			43			
49	RAMAD2			69			
50	RAMAD1	O	High order address signals of the SRAM & MROM.	15	GND	-	Ground pins.
51	RAMAD0			52			
53	RAMA14			72			
54	RAMA13						
55	RAMA12						
56	RAMA11						
57	RAMA10						
58	RAMA9						
59	RAMA8	O	Low address signals of the SRAM & MROM.				
65	RAMA7						
66	RAMA6						
67	RAMA5						
68	RAMA4						
73	RAMA3						
74	RAMA2						

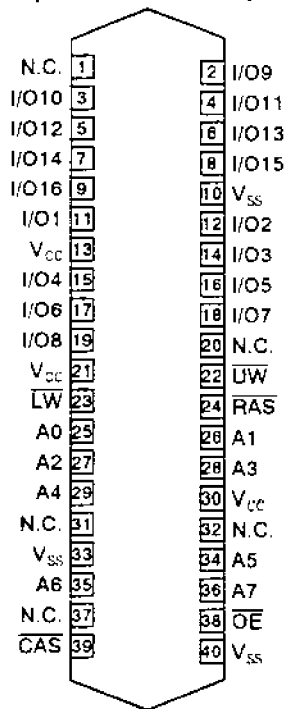
Note: The interface with the serial DAC is formed in the MSB initial mode.

IC 7/8 65536 Word \times 16bit Dynamic RAM

IC TC511664BZ-80

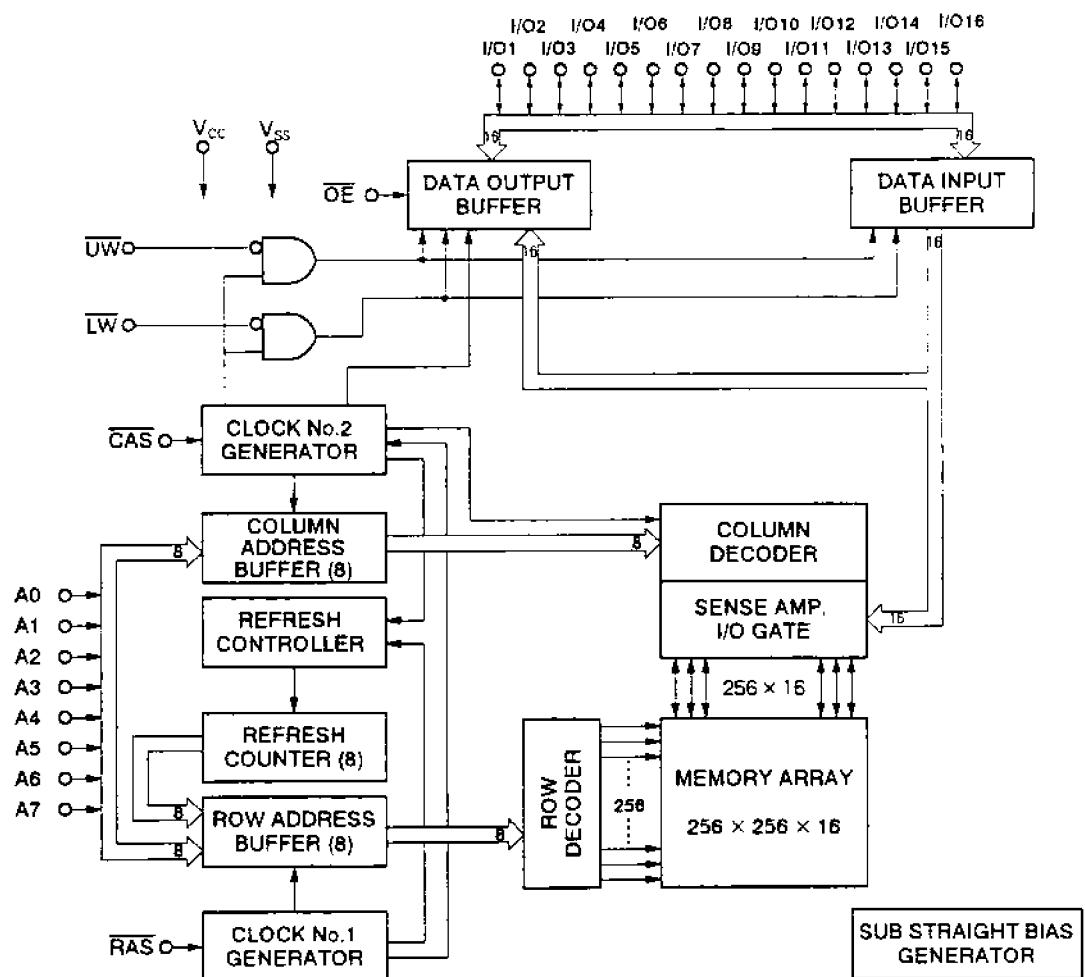
IC TC511664Z80

■ Top View & Pin Layout



■ Pin Name

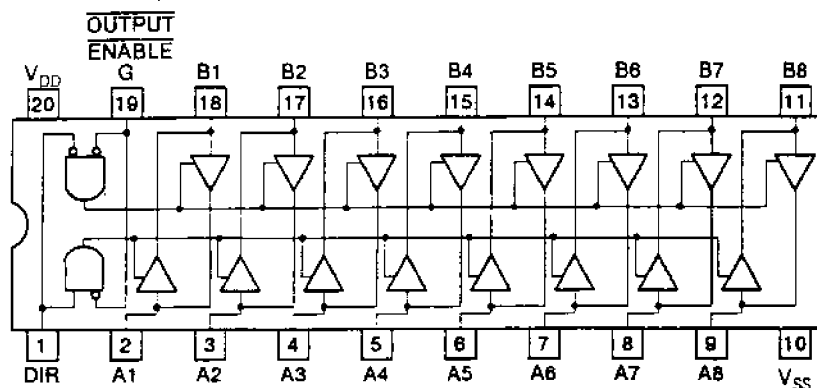
A0-A7	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{UW}}$	Read/Upper Bit Write Input
$\overline{\text{LW}}$	Read/Lower Bit Write Input
$\overline{\text{OE}}$	Output Enable
I/O1-I/O16	Data I/O
V _{CC}	Power Supply (+5V)
V _{SS}	Ground
N.C.	Not Connected



IC9 8-Circuits Non-Inverting Bus Transceiver

IC 74HC245

Top View & Pin Layout

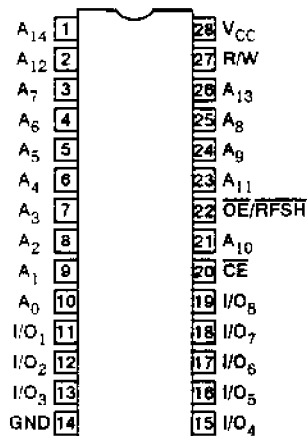


IC10/11 8bit CMOS Pseudo Static RAM

IC TC51832AFL-10

IC TC51832FL-10

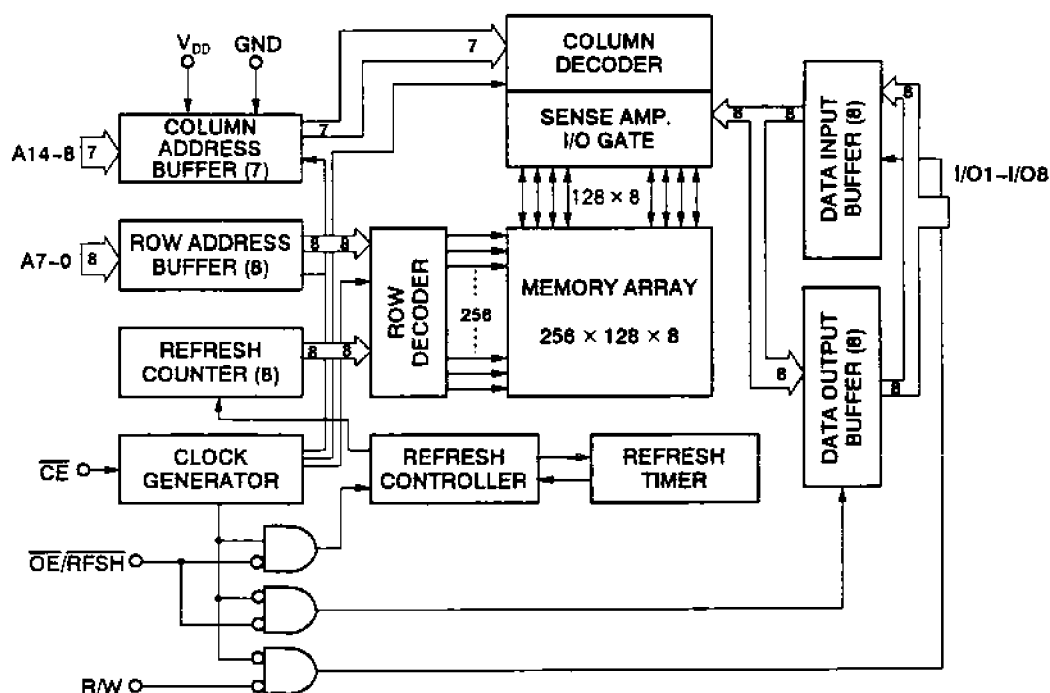
Top View & Pin Layout



Pin Configuration and Pin Description

Symbol	Pin Name
A ₀ -A ₁₄	Address Input
R/W	Read / Write Input
$\overline{\text{OE}}$ / $\overline{\text{RFSH}}$	Output Enable / Refresh
$\overline{\text{CE}}$	Chip Enable
I/O ₁ -I/O ₈	Data Input / Output

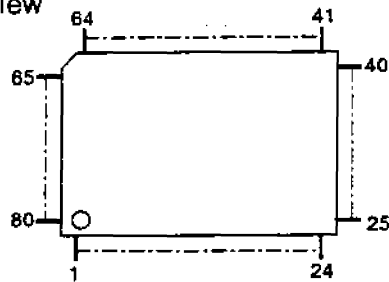
Block Diagram



IC13 CD-ROM LSI

IC LC8951

■ Top View



■ Description

No.	I/O	Pin Name	No.	I/O	Pin Name	No.	I/O	Pin Name	No.	I/O	Pin Name
1	—	V _{SS}	21	I/O	IO3	41	—	V _{SS}	61	O	EOP
2	O	RA6	22	I/O	IO2	42	I/O	D3	62	O	RCS
3	O	RA7	23	I/O	IO1	43	I/O	D4	63	O	HDE
4	O	RA8	24	—	V _{SS}	44	I/O	D5	64	—	V _{SS}
5	O	RA9	25	I	EXTAL	45	I/O	D6	65	I/O	HD7
6	O	RA10	26	O	XTAL	46	I/O	D7	66	I/O	HD6
7	O	RA11	27	I	TEST A	47	I	RS	67	I/O	HD5
8	O	RA12	28	I	TEST B	48	I	RD	68	I/O	HD4
9	O	RA13	29	I	CSEL	49	I	WR	69	I/O	HD3
10	O	RA14	30	I	LMSEL	50	I	CS	70	I/O	HD2
11	O	RA15	31	—	V _{DD}	51	O	INT	71	I/O	HD1
12	O	RWE	32	I	LRCK	52	—	V _{SS}	72	I/O	HD0
13	—	V _{SS}	33	I	SDATA	53	I	RESET	73	—	V _{DD}
14	O	ROE	34	I	BCK	54	I	ENABLE	74	I	SELDRQ
15	I/O	ERA	35	I	C4LR	55	I	HRW	75	O	RA0
16	I/O	IO8	36	I	C2PO	56	I	HRD	76	O	RA1
17	I/O	IO7	37	O	MCK	57	I	CMD	77	O	RA2
18	I/O	IO6	38	I/O	D0	58	O	WAIT	78	O	RA3
19	I/O	IO5	39	I/O	D1	59	O	DTEN	79	O	RA4
20	I/O	IO4	40	I/O	D2	60	O	STEN	80	O	RA5

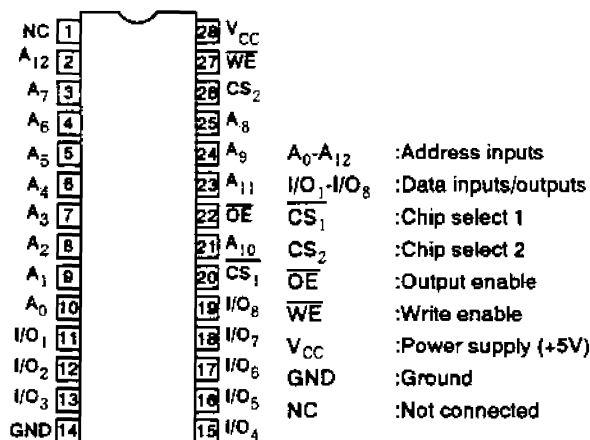
IC14/15/16 64k(8k × 8)bit Static RAM

IC MB8464A-90

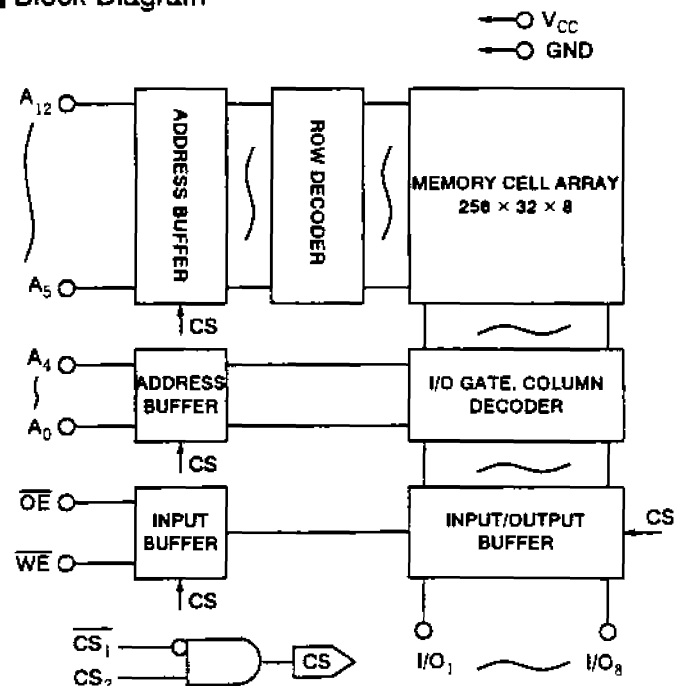
IC MB8464A-80

IC MB8464A-10LL PF-G-BND

■ Top View & Pin Layout



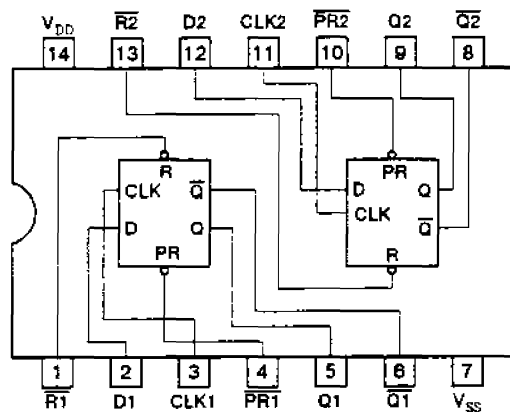
■ Block Diagram



IC17 2-Circuit D-type Flip-flop

IC 74AC74

IC74VHC74

■ Top View & Pin Layout

IC1/2 18Bit Digital Filter & 16Bit D/A Converter

IC LC7881M - C

IC 7883KM

■ Top View

■ Description

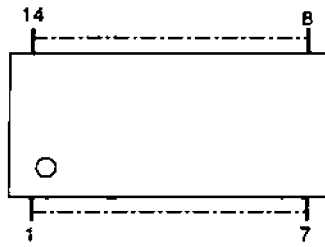
Pin	Name	I/O	Function
1	CH1OUT	O	DAC CH-1 output.
2	VrefH	-	Reference voltage "H" input.
3	AVDD	-	Power supply of analog circuits.
4	DVDD	-	Power supply of digital circuits.
5	BLCK	I	Bit clock.
6	DATA	I	Digital audio data input. Input from the MSB in the bit serial state.
7	LRCK	I	L/R clock input. LRCK= "H" CH1 LRCK= "L" CH2
8	TEST	I	Test pin. (normally, set to "L")
9	ATT	I	Attenuator data input. Input from the LSB in the bit serial state.
10	SHIFT	I	Attenuator data transfer clock input.
11	LATCH	I	Attenuator data latch clock input.
12	INITB	I	Initializing signal input. (normally, set to "H")
13	TEST	I	Test pin. (normally, set to "L")

Pin	Name	I/O	Function
14	EMPH2	I	De-emphasis setting pins.
15	EMPH1		
16	D/N	I	Double/Normal speed switching pin.
17	SOC2	I	Input source select inputs. (PULL-DOWN)
18	SOC1		
19	MODE	I	Operation mode setting pin. (PULL-DOWN)
20	TEST	I	Test pins. (normally, set to "L") (PULL-DOWN)
21			
22	DGND	-	Ground of digital circuits.
23	CLKOUT	O	Clock output. 392Fs: 1/2 XOUT 384Fs, 448Fs, 512Fs : XOUT
24	XIN	I	Crystal oscillator input.
25	XOUT	O	Crystal oscillator output.
26	AGND	-	Ground of analog circuits.
27	VrefL	-	Reference voltage "L" input.
28	CH2OUT	O	DAC CH-2 output.

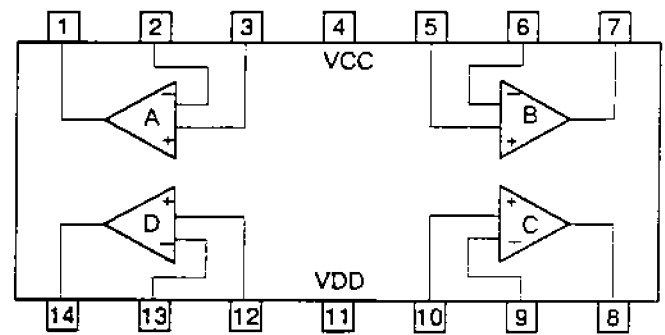
IC3/4/5 Quad Operational Amplifier

IC UPC844G2

■ Top View



■ Pin Layout



IC6 3-Terminal Voltage Regulator

IC UPC2405HF

■ Front View

